In the Claims:

1-21. (canceled)

22. (new) An RF receiver integrated circuit, comprising:

A. a substrate of semiconductor material;

B. mixer circuitry, formed on the substrate, having an input for receiving an analog RF signal with a bandwidth of f_o and an output for supplying an analog IF signal of frequency f_c in response to receiving the analog RF signal;

C. analog to digital converter circuitry, formed on the substrate, having an input connected with the output of the mixer circuitry and having four parallel outputs carrying signals representing a digital IF signal, the converter circuitry having a sampling frequency f_s of four times f_c;

D. CORDIC circuitry, formed on the substrate, having four parallel inputs connected with the four parallel outputs of the converter circuitry, a first set of four outputs, and a second set of four outputs;

E. first decimator and quantizer circuitry, formed on the substrate, having inputs connected with the first set of four outputs and an output of two bits supplying signals at a sampling frequency of $2xf_o$;

F. second decimator and quantizer circuitry, formed on the substrate, having inputs connected with the second set of four outputs and an output of two bits supplying signals at a sampling frequency of $2xf_o$;

G. multiplex and serial to parallel circuitry, formed on the substrate, having inputs connected with the outputs of the first and second decimator and quantizer circuitry and having a serial output; and

H. first differential transmitter circuitry, formed on the substrate, having an input connected with the serial output and having first differential serial outputs for sending signals at a sampling rate of $8xf_o$ from the substrate.

23. (new) The integrated circuit of claim 22 in which the multiplex and serial to parallel circuitry has a clock signal input, and including a clock lead, formed on the substrate, carrying a clock signal at a frequency of $48xf_o$, first divider circuitry having an input connected to the clock lead and an output providing a clock signal at $8xf_o$ connected to the clock signal input of the multiplex and serial to parallel circuitry.

24. (new) The integrated circuit of claim 23 including a second integrated circuit including:

A. first differential receiver circuitry having differential serial inputs connected with the first differential serial outputs and a serial output;

B. serial to parallel converter circuitry having a serial input connected with the serial output of the first differential receiver circuitry and parallel outputs carrying respectively a SIGN1-I signal, a MAG1-I signal, a SIGN1-Q signal, and a MAG1-Q signal, at a frequency of $2xf_o$, and

C. digital communication processing circuitry having inputs connected with the parallel outputs.

25. (new) The integrated circuit of claim 23 including second differential transmitter circuitry, formed on the substrate, having an input connected with the clock lead and having second differential serial outputs for sending clock signals at a sampling rate of $48xf_o$ from the substrate.

26. (new) The integrated circuit of claim 25 including a second integrated circuit including:

A. first differential receiver circuitry having differential serial inputs connected with the first differential serial outputs and a serial output;

B. second differential receiver circuitry having differential serial inputs connected with the second differential serial outputs and a serial output;

C. second divider circuitry having an input connected with the serial output of the second differential receiver circuitry and an output supplying a clock signal at a frequency of $8xf_o$;

D. serial to parallel converter circuitry having a serial input connected with the serial output of the first differential receiver circuitry, a clock input connected with the output of the second divider circuitry, and parallel outputs carrying respectively a SIGN1-I signal, a MAG1-I signal, a SIGN1-Q signal, and a MAG1-Q signal, at a frequency of $2xf_o$; and

D. digital communication processing circuitry having inputs connected with the parallel outputs and a clock input connected with the serial output of the second differential receiver circuitry.